REMARKS

Claims 1, 3 - 8 and 10 - 17 remain active in this application. Claims 2 and 9 have previously been canceled. No new matter has been introduced into the application. The withdrawal of all former rejections, objections and requirements in regard to matters of form in noted with appreciation.

The sole remaining issue in this application is the Examiner's rejection of claims 1, 3 - 8 and 10 - 17 under 35 U.S.C. §102 as being anticipated by Schwartz repeated from prior actions without further comment and referring to *four* prior actions for the Examiner's reasoning. This ground of rejection is again respectfully traversed for the reasons made of record in previous responses which are hereby fully incorporated by reference and the further remarks provided below.

Initially, it was noted in the previous response (page 13, first full paragraph) that the Examiner's statement of the rejection was unclear as to statutory basis due to use of terms such as "unpatentable", "patentably distinct" and "non-obvious" in a rejection made under 35 U.S.C. §102 for anticipation. *No clarification has been made on this issue and the Examiner has incorporated that statement of the rejection by reference in the present action.*

Further in this regard, it is respectfully pointed out that this Request for Reconsideration is in response to the *fifth* action on the merits of this application while the Examiner adheres to a ground of rejection making reference to *four prior* actions and it does not appear that a *prima facie* demonstration of anticipation (or obviousness) has been made to date, as pointed out in the previous response. Accordingly, it is respectfully submitted that close supervisory review is in order under M.P.E.P. §707.02 and is requested.

Additionally in this regard, it was previously noted that substantial confusion as to the nature of the invention was apparent even in the most recent previous action. In response, the invention was summarized in detail in the previous response as follows:

> Built-in self test (BIST) arrangements of many different forms and constitutions are known for performing different tests on various functional sections, such as an embedded memory, of a chip. The types of tests can generally be considered as falling into one of three groups: manufacturing level tests, board level tests and system level tests. Also, in general, external testers can be used for manufacturing level tests and board level tests (e.g. during manufacture of boards or later service and/or repair) but external testers are not generally available for system level tests which must be performed frequently or upon the occurrence of particular operations such as powering up the system in which a chip requiring testing is installed. It should also be appreciated that storage of signals for use by the BIST structure requires space on the chip and is not justified for manufacturing level and board level tests which are not generally performed after the chip is placed in service, particularly in view of the availability of external testers to supply signals for such tests. Thus, for manufacturing level and board level tests the BIST structure often has a principal function of providing access to signal lines necessary for such tests (see page 5, lines 8 - 11 and page 6, lines 16 - 21). On the other hand,

where an external tester is not generally available, as in the case of system level tests (and which are more frequently performed), the inclusion of storage for the test signal patterns on the chip is justified and may be provided by non-volatile storage such as a read only memory (ROM), which may preclude access by an external tester, or small random access memory (RAM); the latter also constituting essentially a further embedded memory which requires testing and which may complicate the test procedure (page 6, lines 3 - 11). Therefore, it is generally preferred to use a register file/instruction storage module 30 (page 6, lines 12 - 16, and page 12, line 30 to page 13, line 4) for manufacturing level and board level testing where an external tester is available for initializing the instruction storage module 30 with a bit string representing the test algorithm and loading instructions for the desired test during the test process (page 6, line 15) even though such an expedient precludes system level test since there no external tester is available as a source of the test algorithm to initialize the instruction storage module 30. Therefore, there is a basic incompatibility between manufacturing and board level tests (collectively referred to as lower level tests) and system level teats (and other tests referred to as higher level tests) where the test instructions are contained in the BIST arrangement and an external tester is unavailable. This incompatibility is aggravated by the severe constraints on efficiency of chip space usage which, as a

practical matter, largely precludes signal connection switching arrangements which may be complex and which must be separately controlled for lower and higher level tests, respectively. Further, while the chip area necessary to accommodate the test instructions for higher level tests may be justified in a BIST arrangement for making such tests, the chip area required to accommodate connection of an external tester must be stringently limited since lower level tests are performed only rarely, if at all, after the chip is placed in service.

To solve this incompatibility consistent with chip area constraints, the invention provides for use of the instruction storage module, preferred for lower level tests, for connection of higher level system test algorithms provided in the BIST arrangement and for internal initialization of the instruction storage module when no initialization signal is available from an external tester or when a particular source of test signals or a particular control signal is discriminated. All that is necessary to perform such a function is to discriminate between lower level tests and higher level tests and to apply an internally generated default initialization signal for higher level tests. The discrimination may be performed efficiently in accordance with the invention by simply determining if a signal applied by an external tester is present since an external tester will be used for lower level tests but not higher level tests. The remainder of the BIST arrangement operation is not affected (page 15, line 18)

and the only operation required is to initialize the instruction storage module when not done in response to signals from an external tester. This operation is completely independent of any structural or operational details of the BIST arrangement and can be performed on any BIST arrangement which uses the much preferred expedient of a file register or instruction storage module.

and

It is abundantly clear in Schwarz that nothing is applied to buffer 206 (the only storage separately disclosed for test signals to be applied to embedded memory 102), other than external data and that any internally generated test signals in Schwarz are not applied thereto. No initialization function is described or suggested in Schwarz but, rather, a substantial difficulty of synchronization is admitted (column 4, lines 15 - 32) since the BIST 104 continues to supply address signals during debugging but no solution is provided. By the same token, it is clear that Schwarz does not and is not directed to providing a solution to any incompatibility between test types since the debugging signals must be made fully compatible with addressing provided by BIST 104. Therefore, it is equally clear that Schwarz does not anticipate any claim is the application and no *prima facie* demonstration of anticipation has been made by the Examiner. Moreover, Schwarz does not provide evidence of a level of ordinary skill in the art which would support a conclusion of obviousness since switching of test signals is performed using multiplexers (which are

relatively complex and consume substantial chip space) under the control of an external signal. Therefore, while it is respectfully submitted that Schwarz is not concerned with extending the *types* of tests which can be performed (e.g. *both* higher and lower level tests) but only adding a debugging facility to locate a source of an error detected in whatever testing is otherwise performed, at best, Schwarz does not provide a solution to the problem addressed by the invention or do so by a simple initialization arrangement for an instruction store otherwise present to address the important constraint on minimizing chip space required for the BIST. Therefore, it is respectfully submitted that no *prima facie* demonstration of obviousness has been or can be made based on Schwarz.

While the issues as to form indicating confusion in regard to the nature of the invention have been withdrawn, the Examiner now asserts that the claims should (or must) be construed broadly enough to be readable on Schwarz. Although the Examiner's summary of Schwarz is substantially correct, it is largely centered upon the "debug" input to multiplexers 202, 204 by which inputs to RAM 102 and comparator 106 can be switched between internal and external sources. However, such an arrangement does not answer the claim recitations and the claim recitations can not be construed broadly enough to be answered by such an arrangement since to do so would effectively ignore explicitly recited distinguishing features of the invention.

Specifically, claims 1 and 8 recite "means for storing test instructions and *discriminating between* performing manufacturing level or board level testing and system level testing based on receiving *test*

instructions provided from an external tester" and claim 17 recites: "*discriminating* a *source* of a *test command*, providing a system level test algorithm from said BIST arrangement *in absence of instructions from an external tester*" (emphasis added). No such *discrimination* of the presence or absence of test instructions from an external tester is or can be taught or suggested in Schwarz for the simple reason that Schwarz must *externally* provide information as to the source of test instructions and control the source from which test instructions are input using multiplexers 202, 204 over the separate "debug" input which is clearly *not* a "test instruction" but a control signal for switching input sources.

Thus even at a most fundamental level and not considering operational differences which have been discussed in previous responses, the invention provides the meritorious effect of avoiding the need to provide space on the chip for two multi-line multiplexers (which is not insignificant since a plurality of transistors are required for *each* input corresponding to *each* line of *each* bus) and the "debug" connection itself (which is not insignificant since the connection requires an external connection pad, an I/O circuit and the additional connection wiring on the chip to control the multiplexers) where chip space for a BIST arrangement must necessarily be stringently limited.

In contrast, the invention *internally* discriminates whether or not a test instruction is present in an existing input circuit such as a buffer prior to initialization of an internal source of test signals and thus determines whether an external tester is present since, at that point (prior to initialization of an internal test signal source), there is no other source of such a signal. If a test signal is not present, the invention supplies a system level test signal from an internal source by

initializing that internal source (which, of course, must be present in any BIST arrangement).

Claims 1 and 8 recite this generation and and supply of *default*, system level test instructions *in response* to the recited *discrimination* as follows:

> "means for generating default test instructions for performing system level testing *when test instructions are not provided by said external tester*, and
>
> "means for *supplying* said default test instructions for performing system level testing *to said means for storing* test instructions,
>
> "wherein *said means for generating default test instructions includes an initialization storage means for providing signals for initializing said means for storing test instructions in the absence of said test instructions provided from an external tester.*" (emphasis added).

The corresponding recitations of claim 17 are:

> "providing a system level test algorithm from said BIST arrangement *in absence of instructions from an external tester*,
>
> "*transferring* said system level test algorithm *to said means for storing a test algorithm* in said BIST arrangement, and
>
> "operating said BIST arrangement using said system level test algorithm." (emphasis added).

Thus, the claims clearly recite 1.) discrimination of the presence or absence of a test instruction and 2.) in response to the discriminated absence of a test instruction supplying a default, system level test instruction/algorithm from an internal source through a means for storing the test instruction or algorithm where the arrangement for supplying the default, system

level test instructions/algorithm and the means for storing it are already necessarily present in any BIST arrangement and the discrimination can be performed very simply with very little additional circuitry (e.g. a single OR gate) and without separate external control where chip space allocated to the BIST arrangement must be held to a minimum.

In asserting that the claims must be construed broadly enough to be readable on Schwarz, the Examiner must necessarily be construing the external "debug" signal as a "test instruction" which it clearly is not, but rather is simply a switching control signal for multiplexers 202, 204. The Examiner then compounds this error by asserting that the assertion or de-assertion of the "debug" signal is a "discrimination" and, further, by glossing over the recitation that the default signals are "generated" in response to the result of the discrimination indicating that no test instruction or algorithm is present as well as the recitation that the default, system level test signal is supplied to a means for storing a test signal (which is otherwise used to receive signals from an external tester). Thus, starting with an erroneous assertion that the "debug" signal is a test instruction, the Examiner effectively misconstrues and/or ignores virtually *all* recitations of the independent claims of the application contrary to the plain meaning of the language of the explicit recitations of the claims. Such a construction is clearly far beyond a "broadest *reasonable*" construction and effectively ignores or dismisses the recited distinguishing features of the invention even at the most fundamental level (e.g. allowing the omission of an *external* connection requiring significant chip space in an environment where efficient chip space usage is particularly critical). In short, nothing in Schwarz is responsive to externally input signals output from buffer 206 to

control generation of internal default test signals, much less any discrimination of the presence or absence of such signals. On the contrary, in Schwarz, internal test signals are generated unconditionally (or at least not controlled in response to the absence of externally appl;ied test instructions) and external signals and corresponding expected data substituted therefor as multiplexers 202, 204, in accordance with an externally applied "debug" signal, engendering a problem of synchronization of external test signals with internally generated addresses (further indicating that operation of BIST 104 is not responsive to the presence or absence of externally applied test signals) which Schwarz explicitly admits. Therefore, Schwarz clearly does not answer the claim recitations and the claim recitations cannot reasonably be construed to be readable on Schwarz: a control signal is not the same as or equivalent to an internal discrimination of the presence or absence of a signal, unconditional internal generation of test signals is not and logically cannot be responsive to such discrimination of the presence or absence of a signal, switching internal signals through a multiplexer is not the same as or equivalent to providing test signals to a storage means provided for storing externally applied signals, etc.; recitations which the Examiner has effectively ignored and which support the meritorious effects of the invention which are not available from Schwarz.

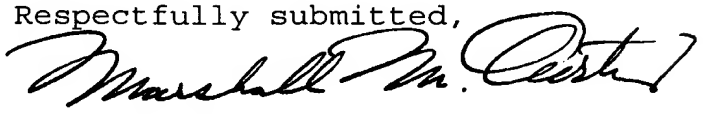
Through such errors, in which the Examiner has long persisted, the Examiner continues to fail to make a *prima facie* demonstration of anticipation of any claim. It is abundant clear that Schwarz does not answer most of the claim recitations and certainly does not anticipate any claim in the application. That the asserted ground of rejection is particularly evident from, *inter alia*, the emphasis placed by the Examiner on the assertion and de-assertion of the "debug" signal

in Schwarz *as* a test instruction or algorithm which it clearly is not, particularly since it is illustrated and described in Schwarz as separate from the signals which are externally input through buffer 206 of Schwarz upon which the claimed discrimination and other claimed functions responsive thereto are based, as claimed. Accordingly, it is respectfully requested that the rejection of claims 1, 3 - 8 and 10 - 17 be reconsidered and withdrawn.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458 of International Business Machines Corporation (E. Fishkill).

Respectfully submitted,



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